Error Detection, Correction LSI for DATA/DAT

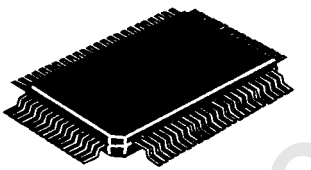
Description

HD49224A is an error detection and correction LSI developed for use in DATA/DAT. It serves as a signal processing section for DATA/DAT when used in conjunction with the HD49227FS. The HD49224A possesses the following characteristics and functions.

Features

- Error correction code processing based on DATA/DAT format
- 5 V single supply
- 2 µm CMOS process for low supply current (150 mW typ)

HD49224A

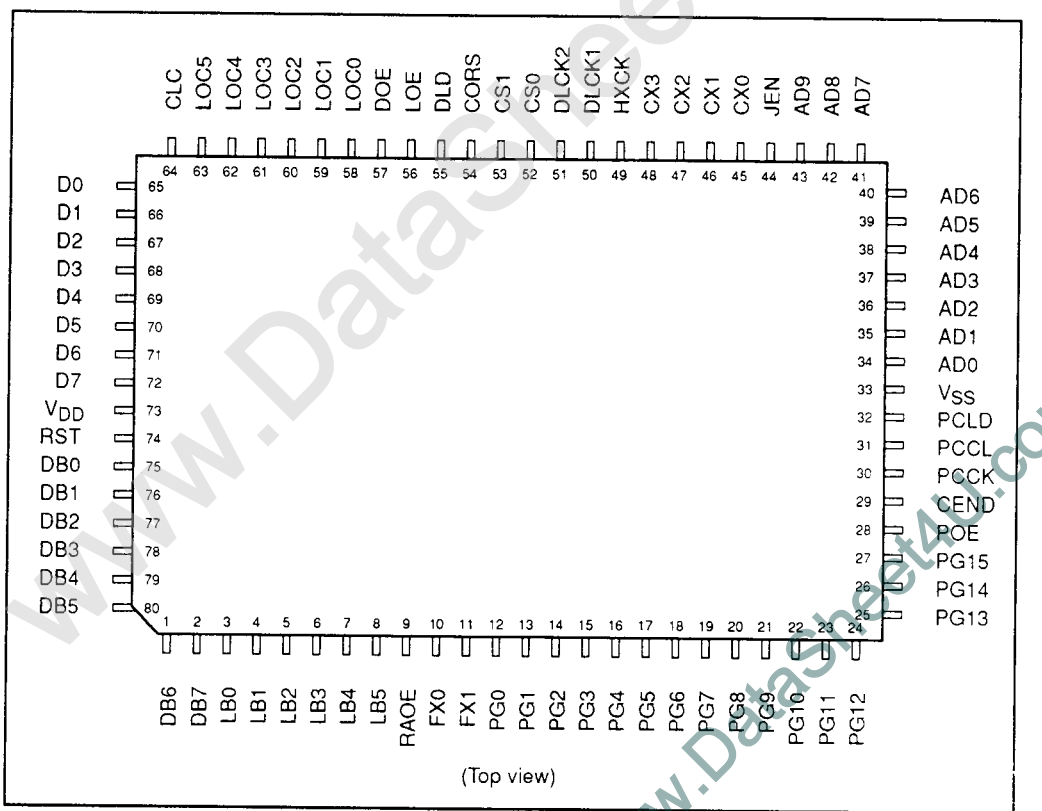


FP-80

Ordering Information

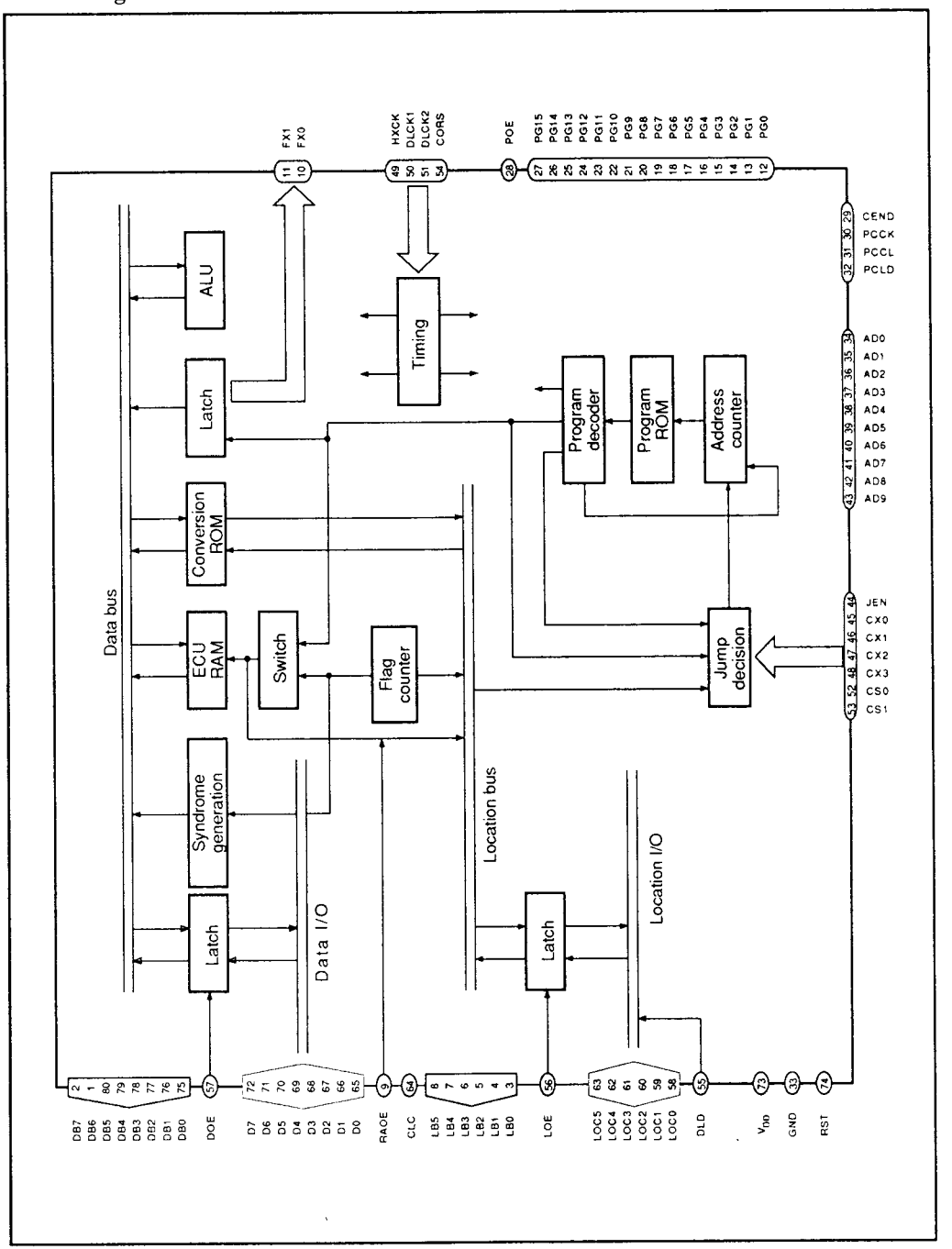
Type No.	Package
HD49224A	FP-80

Pin Arrangement



(Top view)

Block Diagram



Pin Functions

Terminal	Symbol	I/O	Connection	Function	Input level
1	DB6	O		Test pin	
2	DB7	O		Test pin	
3	LB0	O		Test pin	
4	LB1	O		Test pin	
5	LB2	O		Test pin	
6	LB3	O		Test pin	
7	LB4	O		Test pin	
8	LB5	O		Test pin	
9	RAOE	I	Pull up	Test pin	CMOS
10	FX0	O		Error flag status for each correction to cycle	
11	FX1	O			
12	PG0	I/O		Test pin	TTL
13	PG1	I/O		Test pin	TTL
14	PG2	I/O		Test pin	TTL
15	PG3	I/O		Test pin	TTL
16	PG4	I/O		Test pin	TTL
17	PG5	I/O		Test pin	TTL
18	PG6	I/O		Test pin	TTL
19	PG7	I/O		Test pin	TTL
20	PG8	I/O		Test pin	TTL
21	PG9	I/O		Test pin	TTL
22	PG10	I/O		Test pin	TTL
23	PG11	I/O		Test pin	TTL
24	PG12	I/O		Test pin	TTL
25	PG13	I/O		Test pin	TTL
26	PG14	I/O		Test pin	TTL
27	PG15	I/O		Test pin	TTL
28	POE	I	Pull up	Test pin	CMOS
29	CEND	O		Test pin	
30	PCCK	O		Test pin	
31	PCCL	O		Test pin	
32	PCLD	O		Test pin	
33	V_{SS}	—	GND	Power supply	
34	AD0	O		Test pin	
35	AD1	O		Test pin	
36	AD2	O		Test pin	
37	AD3	O		Test pin	
38	AD4	O		Test pin	
39	AD5	O		Test pin	

FX1, FX0	0,0	0,1	1,0	1,1
Correction	OK	—	—	NG

Pin Functions (Cont.)

Terminal	Symbol	I/O	Connection	Function	Input level
40	AD6	O		Test pin	
41	AD7	O		Test pin	
42	AD8	O		Test pin	
43	AD9	O		Test pin	
44	JEN	I	Pull up	Test pin	CMOS
45	CX0	I	μ-com	Program encode/decode control signal "L" = decode mode	CMOS
46	CX1	I	HD49227FS	Format ID 0/1 control "L": format ID = 0	CMOS
47	CX2	I	GND	Test pin	CMOS
48	CX3	I	GND	Test pin	CMOS
49	HXCK	I		Master clock 24.576 MHz	CMOS
50	DLCK1	I	HD49227FS	Control signal latch clock Used by CS0, CS1, CX0, CX1, CX2, CX3, CORS, DLD latches	CMOS
51	DLCK2	I	HD49227FS	Data I/O (D0 to D7), location I/O (LOC0 to LOC5) latch signal	CMOS
52	CS0	I	HD49227FS	Program control signal CS0 0 1 Mode DATA FLAG	CMOS
53	CS1	I	GND		
54	CORS	I	HD49227FS	Encode, decode start signal Starts at rise	CMOS
55	DLD	I	HD49227FS	Data input control signal "H" generates data input syndrome	CMOS
56	LOE	I	HD49227FS	Location I/O control "H" = output	CMOS
57	DOE	I	HD49227FS	Data I/O control "H" = output	CMOS
58	LOC0	I/O	HD49227FS	Location I/O (LSB) Address signal of RAM being input to/output from by ECU	CMOS
59	LOC1	I/O	HD49227FS	Location I/O Address signal of RAM being input to/output from by ECU	CMOS
60	LOC2	I/O	HD49227FS	Location I/O Address signal of RAM being input to/output from by ECU	CMOS
61	LOC3	I/O	HD49227FS	Location I/O Address signal of RAM being input to/output from by ECU	CMOS
62	LOC4	I/O	HD49227FS	Location I/O Address signal of RAM being input to/output from by ECU	CMOS
63	LOC5	I/O	HD49227FS	Location I/O Address signal of RAM being input to/output from by ECU	CMOS

Pin Functions (Cont.)

Terminal	Symbol	I/O	Connection	Function	Input level
64	CLC	I	Pull up	Test pin	CMOS
65	D0	I/O	HD49227FS RAM	Data I/O (LSB)	TTL
66	D1	I/O	HD49227FS RAM	Data I/O	TTL
67	D2	I/O	HD49227FS RAM	Data I/O	TTL
68	D3	I/O	HD49227FS RAM	Data I/O	TTL
69	D4	I/O	HD49227FS RAM	Data I/O	TTL
70	D5	I/O	HD49227FS RAM	Data I/O	TTL
71	D6	I/O	HD49227FS RAM	Data I/O	TTL
72	D7	I/O	HD49227FS RAM	Data I/O (MSB)	TTL
73	V_{DD}	—	+5 V	Power supply	
74	RST	I	Pull up	Master reset	CMOS
75	DB0	O		Test pin	
76	DB1	O		Test pin	
77	DB2	O		Test pin	
78	DB3	O		Test pin	
79	DB4	O		Test pin	
80	DB5	O		Test pin	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to +7	V
Terminal voltage	V_T	−0.3 to V_{DD} + 0.3	V
Maximum power dissipation	P_T	400	mW
Operating temperature	Topr	−20 to +75	°C
Storage temperature	Tstg	−55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Electrical Characteristics (V_{SS} = 0 V, Ta = 25°C)

		Symbol	Min	Typ	Max	Unit	Test condition	Applicable terminal
Supply voltage		V_{DD}	4.5	5.0	5.5	V		V_{DD}
Input voltage (1)	"H" level	V_{IH1}	0.7 × V_{DD}	—	—	V		CMOS
	"L" level	V_{IL1}	—	—	0.3 × V_{DD}	V		
Input voltage (2)	"H" level	V_{IH2}	2.3	—	—	V	V_{DD} = 5 V ± 10%	TTL
	"L" level	V_{IL2}	—	—	0.6	V	V_{DD} = 5 V ± 10%	
Input leak current		I_{L1}	—	—	1	μA	$0 \le V_I \le V_{DD}$	
Input terminal pull up resistance		Rpu	10 k	—	40 k	Ω		*1
Output voltage	"H" level	V_{OH}	V_{DD} − 0.5	—	—	V	$-I_{OH}$ = 0.4 mA	
	"L" level	V_{OL}	—	—	0.4	V	I_{OL} = 0.4 mA	

Note: 1. POE, JEN, CLC, RST, RAOE